IR-2541 DIV (2-3590)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF APPEALS AND INTERFERENCES

In re Patent Application of	New York, New York
Daniel M. Kinzer et al.	Date: February 23, 2009
Serial No.: 10/613,326	Group Art Unit: 2811
Filed: July 3, 2003	Examiner: Ori Nadav

For: VERTICAL CONDUCTION FLIP-CHIP DEVICE WITH BUMP CONTACTS ON SINGLE SURFACE

VIA EFS-WEB
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF PURSUANT TO 37 C.F.R. §41-31

Sir:

This appeal is from the Examiner's final rejection of this application dated August 25, 2008.

I. REAL PARTY IN INTEREST

The real party in interest in the above-identified application is:

International Rectifier Corporation

II. RELATED APPEALS AND INTERFERENCES

The applicant(s), the assignee(s) and the undersigned attorneys are not aware of any related appeals and interferences.

III. STATUS OF CLAIMS

Claims 1, 3-4, 8-10, 12, 14-17, 19, and 27-29 are pending and on appeal herein.

Claims 2, 5-7, 11, 13, 18, and 20-26 have been canceled.

IV. STATUS OF AMENDMENTS

No Amendment has been filed since the Final Rejection.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The present invention is directed at a semiconductor device, and more particularly a power semiconductor device, which is configured for flip chip mounting (See spec., page 2, lines 8-10, spec., page 5, lines 2-5). That is, a device according to the present invention as claimed has one surface (see Fig. 4, top surface of die 30, spec., page 5, lines 2-15) which includes electrodes (source and drain electrodes 31, 32) for power connection as well as an electrode (gate electrode 33) for receiving control signals. More specifically, the claimed device is a power MOSFET (spec., page 5, line 3) which includes a source electrode, a drain electrode, and a gate electrode on a first major surface thereof (spec., page 5, lines 12-15).

Provided below are the currently pending claims that include citations to the specification and or the figures as a summary of the claimed subject matter pursuant to 37 C.F.R. §41.37(c)(1)(v).

1. (Previously Presented) A flip chip semiconductor device (spec., page 5, line 3) comprising a silicon wafer (Fig. 4, 30, page 5, line 13, lines 19-20) having parallel first and second major surfaces (e.g. Fig. 4, top and bottom surfaces of silicon wafer 30 respectively); at least one P region (e.g. region 51 in Fig. 4) and at least one N region (e.g. region 52 in Fig. 4) in said wafer (30) which meet at a PN junction (regions 51 and 52 meet at a PN junction) within said silicon wafer (30); first and second laterally spaced and metallized layers (metallized layers 31, 32 in Fig. 4) formed on said first major surface (top surface) and each connected to one of said P region and said N region (e.g. metallized layer 31 connected to region 52 through contact openings 81, 82 and N^+ regions at the bottom thereof, and metallized layer 32 connected to region 51 though connection to region 50); a bottom metallized layer extending across said second major surface (spec., page 8, lines 3-5); and

a third metallized layer (gate pad 33, Fig. 2) atop said first major surface which is laterally spaced from said first and second metallized layers (31,32); said first, second and third

metallized layers comprising source, drain and gate electrodes (spec., page 6, lines 14-15) respectively of a MOSgated device (spec., page 5, line 21), wherein a current path inside said silicon wafer from said source electrode to said drain electrode includes a vertical component which is generally perpendicular to said first major surface (spec., page 7, lines 7-14, where it is disclosed that current travels adjacent gate oxide layers 70-74 which are vertically oriented, laterally through region 50, and vertically toward drain electrode 31).

12. (Previously Presented) A flip chip semiconductor device (spec., page 5, line 3) comprising a silicon wafer (Fig. 4, 30, page 5, line 13, lines 19-20) having first and second parallel major surfaces (e.g. Fig. 4, top and bottom surfaces of silicon wafer 30 respectively); at least one P region (e.g. region 51 in Fig. 4) and at least one N region (e.g. region 52 in Fig. 4) in said wafer (30) which meet at a PN junction (regions 51 and 52 meet at a PN junction) within said silicon wafer (30); first and second laterally spaced metallized layers (metallized layers 31, 32 in Fig. 4) formed on said first major surface (top surface) and each connected to one of said P region and said N region (e.g. metallized layer 31 connected to region 52 through contact openings 81, 82 and N^+ regions at the bottom thereof, and metallized layer 32 connected to region 51 though connection to region 50); a third metallized layer (gate pad 33, Fig. 2) atop said first major surface which is laterally spaced from said first and second metallized layers (31,32); said first, second and third metallized layers comprising source, drain and gate electrodes (spec., page 6, lines 14-15) respectively of a MOSgated device (spec., page 5, line 21); and a plurality of contact bumps connected to each of said first and second metallized layers (see Figs. 9, 10, and spec., page 8, lines 6-15); said plurality of contact bumps connected to said first metallized layer being aligned along a first straight row (see Fig. 10); said plurality of contact bumps connected to said second metallized layer being aligned along a second straight row (see Fig. 10), wherein a current path inside said silicon wafer from said source electrode to said drain electrode includes a vertical component which is generally perpendicular to said first major surface (spec., page 7, lines 7-14, where it is disclosed that current travels adjacent gate oxide layers 70-74, laterally through region 50, and vertically toward drain electrode 31).

16. (Previously Presented) The device of claim 12, wherein said first and second rows are parallel to one another (see Fig. 10, spec., page 8, line 13).

17. (Previously Presented) The device of claim 12, wherein said silicon wafer is a rectangular wafer having an area defined by a given length and a given width, said length being greater than said width; said first and second rows of bumps being parallel to one another and being symmetric about a diagonal line across said wafer (see Fig. 14, spec., page 9, line 13 - page 10, line 3).

27. (Previously Presented) A semiconductor device (Fig. 4 and spec., page 5, line 3) comprising a silicon die (Fig. 4, 30, page 5, line 13, lines 19-20) having first and second parallel surfaces (e.g. top and bottom surfaces of wafer 30); a region (region 51) of one conductivity type (e.g. p-type) extending from said first surface and into the body of said die; a junction pattern defined in said device formed by a plurality of laterally spaced diffusions (region 52 which is divided into spaced diffusions by gate trenches) of the other conductivity type into said region of one conductivity type (51); a first conductive power electrode (31) formed atop said first surface and in contact with said plurality of laterally spaced diffusions (electrode 31 makes contact to the diffusions through openings 81 and 82 and makes electrical contact within the diffusions through N^+ regions); a second conductive power electrode (32) formed atop said first surface which is laterally spaced from said first conductive electrode (31) and in electrical contact with the body of said die through a high conductivity element (see Figs. 7 and 8, and spec., page 7, lines 1-6); and at least one solder ball connector formed atop each of said first and second conductive electrodes respectively (see Figs. 1-3, 40-43, spec., page 5, lines 16-20); the current path inside said silicon die from said first conductive electrode to said second conductive electrode having a vertical component which is generally perpendicular to said first surface (spec., page 7, lines 7-14, where it is disclosed that current travels adjacent gate oxide layers to 74, which is a vertical path, laterally through region 50, and again vertically toward drain electrode 31).

28. (Original) A semiconductor device according to claim 27, wherein said high conductivity element is a sinker diffusion of higher conductivity than said body region (Fig. 8, spec., page 7, lines 1-5).

29. (Original) A semiconductor device according to claim 27, wherein said high conductivity element is a metallic material residing in a trench formed in said body of said die (Fig. 8, spec., page 7, lines 5-6).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Whether claims 1, 12, and 27 were properly rejected under 35 U.S.C. §112, first paragraph.

Whether claims 1, 12, and 27 were properly rejected under 35 U.S.C. §112, second paragraph.

Whether claims 1, 12, 16-17, and 27-29 were properly rejected under 35 U.S.C. §103(a) as obvious over Nakagawa et al., (Nakagawa), U.S. Patent No. 5,105,243 in view of Coe et al. (Coe), U.S. Patent No. 5,128,730, and in further view of Rinne et al., (Rinne), U.S. Patent No. 6,117,299.

VII. ARGUMENT

A. Rejection of Claims 1, 12, and 27 under 35 U.S.C. §112, first paragraph

The Examiner has alleged that there is no support for a current path from a source electrode to a drain electrode that includes a vertical component.

It is respectfully submitted that Fig. 4, and the specification at page 7, lines 7-13, disclose a current path that includes vertical portions along gate oxide layers 70 to 74 and "upwardly" through regions 90 or 92 to drain electrode 31. Thus, there is adequate support for the limitations set forth in claims 1, 12 and 27.

The Examiner further alleges that there is no support "first and second laterally spaced and metallized layers each connected to one of said P region and said N region".

Fig. 4 illustrates a P region 51 to which drain electrode 32 is connected through region 50, and an N region 52 formed in P region 51 to which source electrode 31 is connected through an N^+ region at bottom of openings 81, 82. Thus, Fig. 4 illustrates a PN junction (junction of regions 51, 52) to which drain and source electrodes are connected as recited in the claims.

Thus, it is respectfully submitted that the specification and the figures adequately support claims 1, 12, and 27.

B. Rejection of Claims 1, 12, and 27 under 35 U.S.C. §112, second paragraph

The Examiner has alleged that claims 1, 12, and 27 are "unclear as to how the respective electrodes can be formed on one first major surface, and at the same time have a vertical component which is generally perpendicular to said first major surface".

However, claims 1, 12, and 27 do not call for the electrodes to have a vertical component. Rather, claims 1, 12, and 27 call for the current path to have a vertical component. Therefore, claims 1, 12, and 27 are in compliance with section 112, second paragraph.

C. Rejection of Claims 1, 12, and 27 under 35 U.S.C. §103(a)

The Examiner states the following regarding Nakagawa:

> Nakagawa et al., teach in figure 2 and related text a semiconductor device comprising a silicon wafer having parallel first and second major surfaces; at least one P region 16 and at least one N region 10 in the wafer which meet at a PN junction within the silicon wafer; first 24 and second 26 laterally spaced and electrode layers formed on the first major surface and each connected to one of said P region and said N region; a bottom electrode layer 14 extending across the second major surface; and
>
> a third electrode layer 22 atop the first major surface which is laterally spaced from the first and second layers; the first, second and third layers comprising source, drain and gate electrodes respectively of a MOS gated device,
>
> wherein a current path inside said silicon wafer from said source electrode to said drain electrode includes a vertical component which is generally perpendicular to said first major surface (since Nakagawa et al. teach an electrode 14 located on the second major surface of the device, or inherently therein).

However, in Nakagawa the current path between source electrode 24, and drain electrode 26 which includes a channel under gate 22 extends laterally between source electrode 24 and drain electrode 26. See Col. 3, lines 46-65. Thus, the current path between source electrode 24 and drain electrode 26 does not include a vertical component.

Furthermore, even assuming that electrode 14 functions as a drain electrode, there will be no current path between a source electrode and a drain electrode located on the same surface that includes a vertical component. Rather, in this hypothetical, there will be a current path between electrodes on opposite surfaces that includes a vertical component. Therefore, Nakagawa does not teach or suggest a device having a current path between a source electrode and a drain electrode on the same surface, the current path having a vertical component.

Coe and Rinne also fail to teach such a feature. Therefore, the combination of Nakagawa, Coe, and Rinne does not render claims 1, 12, and 27 obvious.

D. Rejection of claim 16 under 35 U.S.C. §103(a)

Claim 16 calls for the rows of contact bumps connected to first and second metallized layers to be parallel to one another.

It has been alleged that Fig. 3 of Rinne teaches such an arrangement. However, Fig. 3 of Rinne teaches a plurality of contact bumps arranged rather randomly. Furthermore, Rinne does not teach or suggest parallel rows of contact bumps connected to respective first and second power electrodes formed atop a first surface of a semiconductor device. Thus, the combination of Nakagawa, Coe and Rinne does not render claim 16 obvious.

E. Rejection of Claim 17 under 35 U.S.C. §103(a)

In support of the rejection of claim 17, the Office Action states that "Nakagawa et al. teach in figure 2 and related text a silicon wafer is a rectangular wafer having an area defined by a given length and a given width, the length being greater than the width. Prior art's device comprises said first and second rows of bumps being parallel to one another and being symmetric about a diagonal line across the wafer."

Fig. 2 of Nakagawa, however, only teaches the cross-section of a device, not an area defined by a length and a width. Furthermore, as explained above, Rinne does not teach parallel bumps connected to respective power electrodes. In addition, Rinne only teaches a random pattern for contact bumps, and not necessarily a symmetric pattern. Therefore, the art of record does not render claim 17 obvious.

F. Rejection of Claim 28 under 35 U.S.C. §103(a)

Regarding the rejection of claim 28, it has been asserted that "Nakagawa et al. teach in figures 6-8 and related text a high conductivity element sinker located outside said region of one conductivity type and has higher conductivity than said body region."

The Office Action does not specify where a sinker can be found in Figs. 6-8. Furthermore, no feature resembling a sinker is readily apparent in Figs. 6-8. Thus, it is respectfully submitted that Nakagawa does not show the features set forth in claim 28. Therefore, claim 28 should not be deemed obvious over Nakagawa, Coe, and Rinne.

G. Rejection of claim 29 under 35 U.S.C. §103(a)

Regarding claim 29 it has been stated that "Nakagawa et al. do not teach said high conductivity element is a metallic material residing in a trench formed in said body of said die. It would have been obvious to one having ordinary skill in the art at the time the invention was made to use a high conductivity element being a metallic material residing in a trench formed in said body of said die in Nakagawa et al.'s device in order to have better control over conductivity and the electrical characteristics of the high conductivity element."

No evidence, however, has been cited to establish that the provision of a metallic material in a trench 25 called for by claim 29 would result in "better control over conductivity and the electrical characteristics of the high conductivity element" in a device disclosed by Nakagawa. Therefore, the record lacks evidence to establish a prima facie case of obviousness against claim 29.

H. Rejection of claims 3, 4, 8, 9, 10, 14, 15, and 19 under 35 U.S.C. §103(a)

Each of claims 3, 4, 8, 9, 10, 14, 15, and 19 depends from one of claims 1 and 12, and, therefore, includes the limitations thereof, as well as, additional limitations which in combination with those of its base chain are not taught or suggested by the art of record. It is respectfully submitted, therefore, that claims 3, 4, 8, 9, 10, 14, 15 and 19 should also be deemed patentable over the art of record.

VIII. CONCLUSION

Claims submitted herein for consideration on appeal should be deemed patentable.

If this communication is filed after a shortened statutory time period has elapsed and no separate Petition is enclosed, the Commissioner of Patents and Trademarks is petitioned, under 37 C.F.R. §1.136(a), to extend the time for filing a response to the outstanding Office Action by the number of months which will avoid abandonment under 37 C.F.R. §1.135. The fee under 37 C.F.R. §1.17 should be charged to our Deposit Account No. 15-0700.

In the event the actual fee is greater than the payment submitted or is inadvertently not enclosed or if any additional fee during the prosecution of this application is not paid, the Patent Office is authorized to charge the underpayment to Deposit Account No. 15-0700.

Respectfully submitted,

THIS CORRESPONDENCE IS BEING SUBMITTED ELECTRONICALLY THROUGH THE UNITED STATES PATENT AND TRADEMARK OFFICE EFS FILING SYSTEM ON February 23, 2009

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CLAIMS APPENDIX

1. (Previously Presented) A flip chip semiconductor device comprising a silicon wafer having parallel first and second major surfaces; at least one P region and at least one N region in said wafer which meet at a PN junction within said silicon wafer; first and second laterally spaced and metallized layers formed on said first major surface and each connected to one of said P region and said N region; a bottom metallized layer extending across said second major surface; and

a third metallized layer atop said first major surface which is laterally spaced from said first and second metallized layers; said first, second and third metallized layers comprising source, drain and gate electrodes respectively of a MOSgated device, wherein a current path inside said silicon wafer from said source electrode to said drain electrode includes a vertical component which is generally perpendicular to said first major surface.

2. (Canceled)

3. (Original) The device of claim 1 which further includes at least one contact bump connected to each of said metallized layers.

4. (Previously Presented) The device of claim 1 which further includes at least one contact bump connected to each of said metallized layers.

5. - 7. (Canceled)

8. (Original) The device of claim 4 wherein said bottom metallized layer is substantially thicker than all of said first and second metallized layers.

9. (Previously Presented) The device of claim 1 wherein a plurality of contact bumps are connected to each of said first and second metallized layers; said plurality of contact bumps connected to said first metallized layer being aligned along a first straight row; said plurality of contact bumps connected to said second metallized layer being aligned along a second straight row.

10. (Original) The device of claim 9 wherein said first and second rows are parallel to one another.

11. (Canceled)

12. (Previously Presented) A flip chip semiconductor device comprising a silicon wafer having first and second parallel major surfaces; at least one P region and at least one N region in said wafer which meet at a PN junction within said silicon wafer; first and second laterally spaced metallized layers formed on said first major surface and each connected to one of said P region and said N region; a third metallized layer atop said first major surface which is laterally spaced from said first and second metallized layers; said first, second and third metallized layers comprising source, drain and gate electrodes respectively of a MOSgated device; and a plurality of contact bumps connected to each of said first and second metallized layers; said plurality of contact bumps connected to said first metallized layer being aligned along a first straight row; said plurality of contact bumps connected to said second metallized layer being aligned along a second straight row, wherein a current path inside said silicon wafer from said source electrode to said drain electrode includes a vertical component which is generally perpendicular to said first major surface.

13. (Canceled)

14. (Previously Presented) The device of claim 12, further comprising a bottom metallized layer extending across said second major surface.

15. (Previously Presented) The device of claim 14, wherein said bottom metallized layer is substantially thicker than all of said first and second metallized layers.

16. (Previously Presented) The device of claim 12, wherein said first and second rows are parallel to one another.

17. (Previously Presented) The device of claim 12, wherein said silicon wafer is a rectangular wafer having an area defined by a given length and a given width, said length being greater than said width; said first and second rows of bumps being parallel to one another and being symmetric about a diagonal line across said wafer.

18. (Canceled)

19. (Previously Presented) The device of claim 14, wherein said silicon wafer is a rectangular wafer having an area defined by a given length and a given width, said length being greater than said width; said first and second rows of bumps being parallel to one another and being symmetric about a diagonal line across said wafer.

20.-26. (Canceled)

27. (Previously Presented) A semiconductor device comprising a silicon die having first and second parallel surfaces; a region of one conductivity type extending from said first surface and into the body of said die; a junction pattern defined in said device formed by a plurality of laterally spaced diffusions of the other conductivity type into said region of one conductivity type; a first conductive power electrode formed atop said first surface and in contact with said plurality of laterally spaced diffusions; a second conductive power electrode formed atop said first surface which is laterally spaced from said first conductive electrode and in electrical contact with the body of said die through a high conductivity element; and at least one solder ball connector formed atop each of said first and second conductive electrodes respectively; the current path inside said silicon die from said first conductive electrode to said second conductive electrode having a vertical component which is generally perpendicular to said first surface.

28. (Original) A semiconductor device according to claim 27, wherein said high conductivity element is a sinker diffusion of higher conductivity than said body region.

29. (Original) A semiconductor device according to claim 27, wherein said high conductivity element is a metallic material residing in a trench formed in said body of said die.

EVIDENCE APPENDIX

None.

RELATED PROCEEDINGS APPENDIX

None.